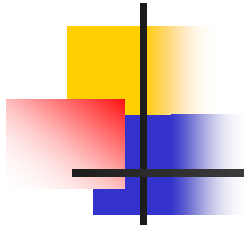


Professional H.264/AVC CODEC Chip-set for High-quality HDTV Broadcast Infrastructure and High-end Flexible CODEC Systems

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Inamori, Takeshi Yoshitome, Hiroaki Matsuda, Ryuichi Tanida,
Atsushi Shimizu, Ken Nakamura, and Jiro Naganuma**

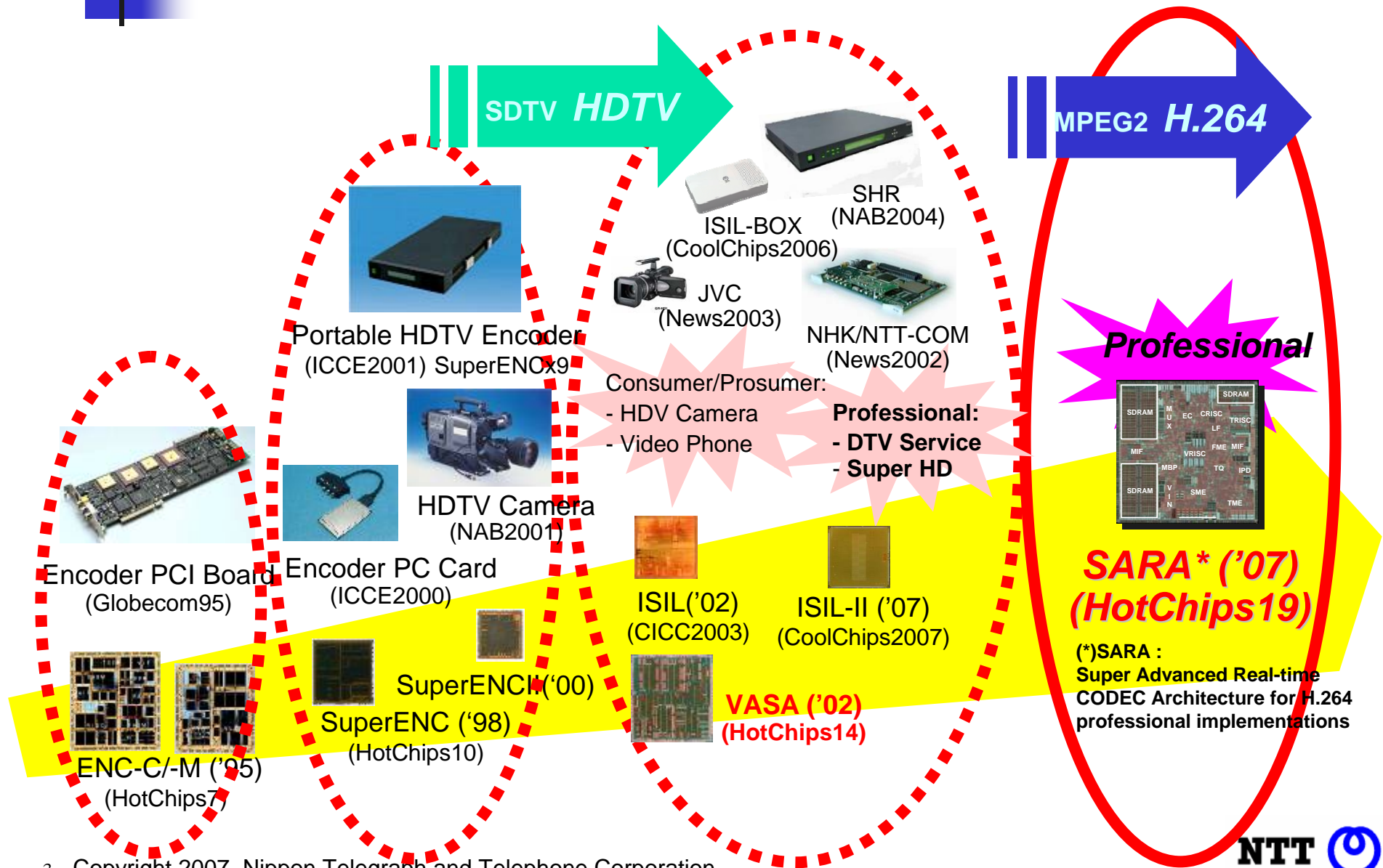
**NTT Cyber Space Laboratories
Nippon Telegraph and Telephone Corporation
Japan**



Outline

- History of NTT's Video CODEC Chips
- Background and Motivation
- What is HDTV Broadcast Infrastructure
- SARA Key Features and Functions
- SARA Main Architecture
- SARA Chip Implementation
- SARA High-end Flexible CODEC Systems
- Summary

History of NTT's Video CODEC LSIs

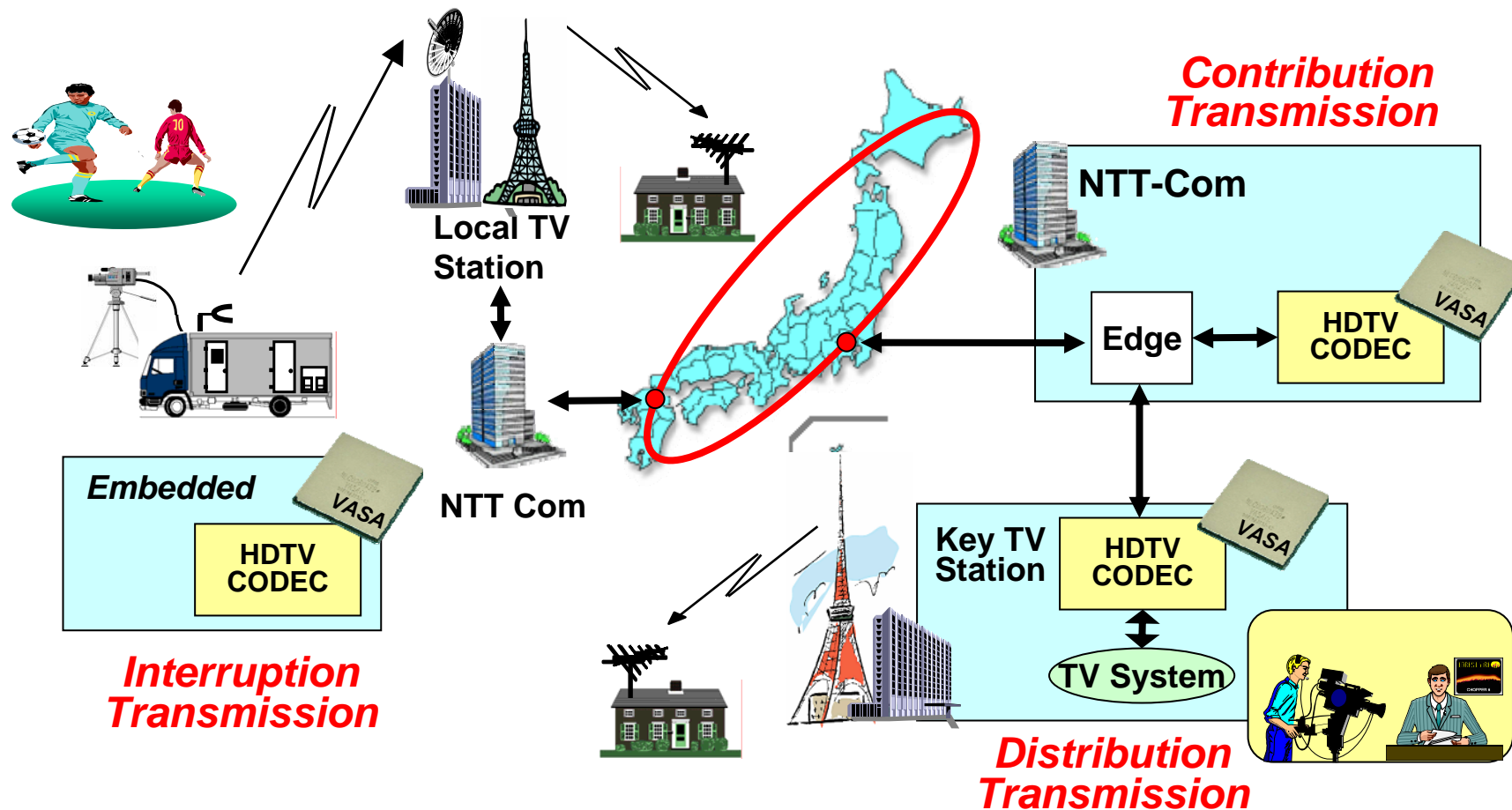


Background and Motivation

- Global wave of H.264 technologies for high efficiency video coding of various HDTV applications.
 - Storage: BD, HD-DVD, AVCHD of optical disc and video camera for consumer.
 - Broadcasting: future digital broadcastings of several countries with Europe DVB-H, Japanese ISDB-T, and US-ATSC have been scheduled already.
 - Main carriers in the world, NTT also, have announced IP-based visual services, IPTV, VOD, and re-transmission of airwave, via IP-broadband network.
- Available chips are ...
 - Domino[X], Ambarella, SONY, Fujitsu, ... for consumer,
 - Telairity (processor-based) for professional (Hot Chips17) and so on.
- *There are few chips with sufficient performance and flexibility for professional applications.*
- ➡ ***SARA: Professional H.264/AVC CODEC Chip-set for HDTV Broadcast Infrastructure and High-end Flexible CODEC Systems.***

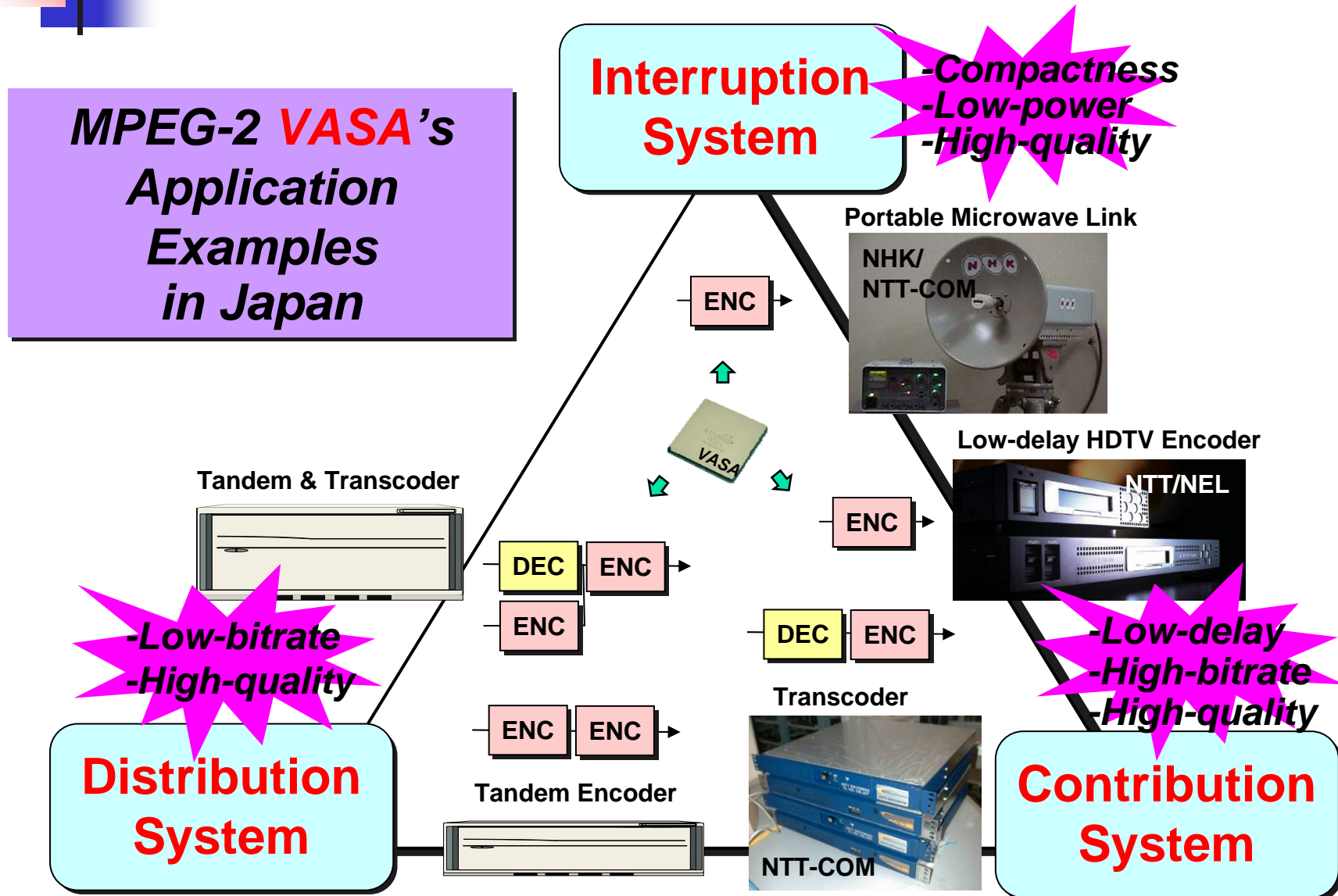
What is HDTV Broadcast Infrastructure

*Digital TV Broadcasting Network Service (NTT Communications)
-- HDTV Transmission network for terrestrial digital broadcasting in Japan --*



➡ **Various High-end CODEC Systems**

Various High-end CODEC Systems

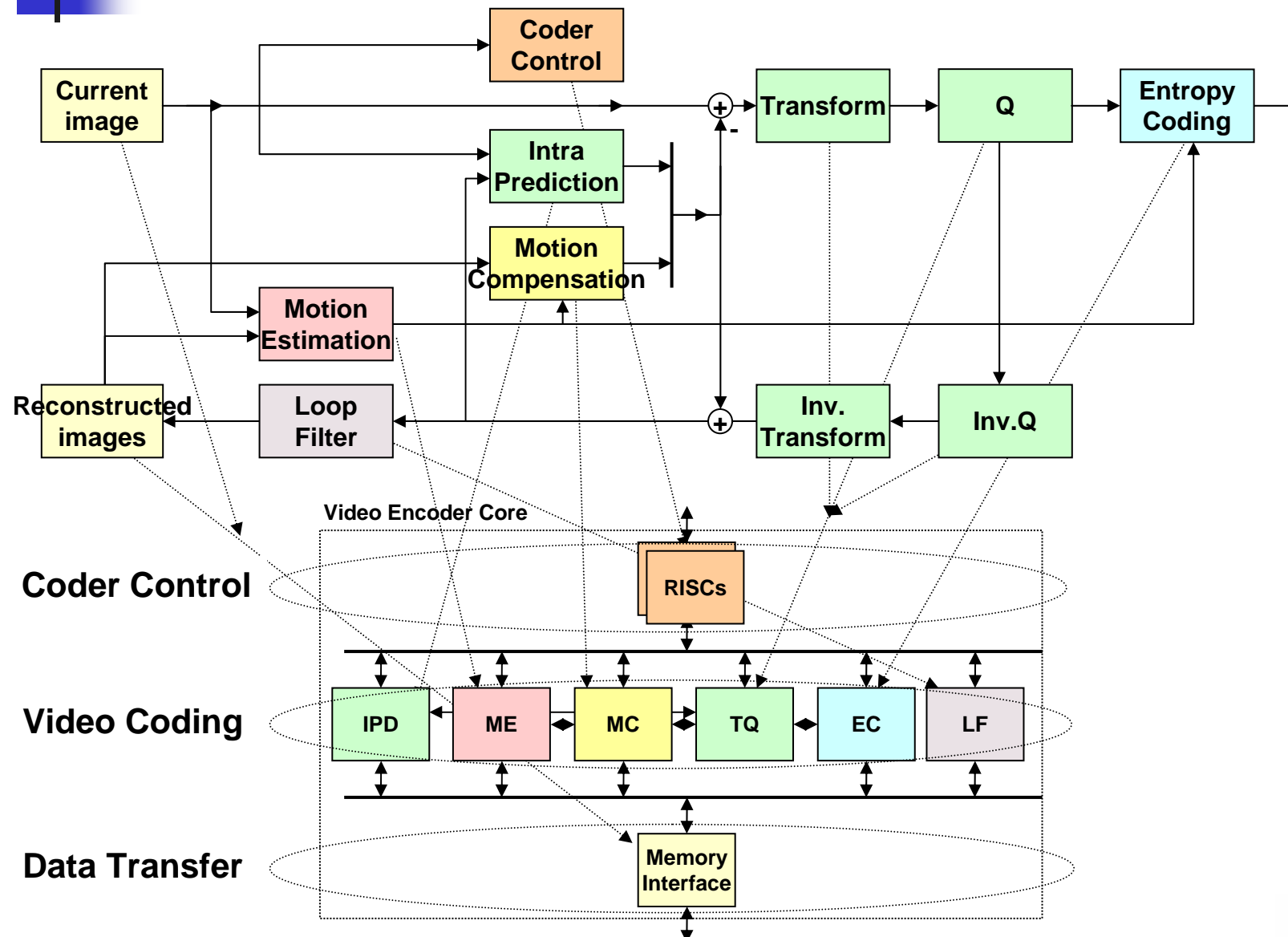




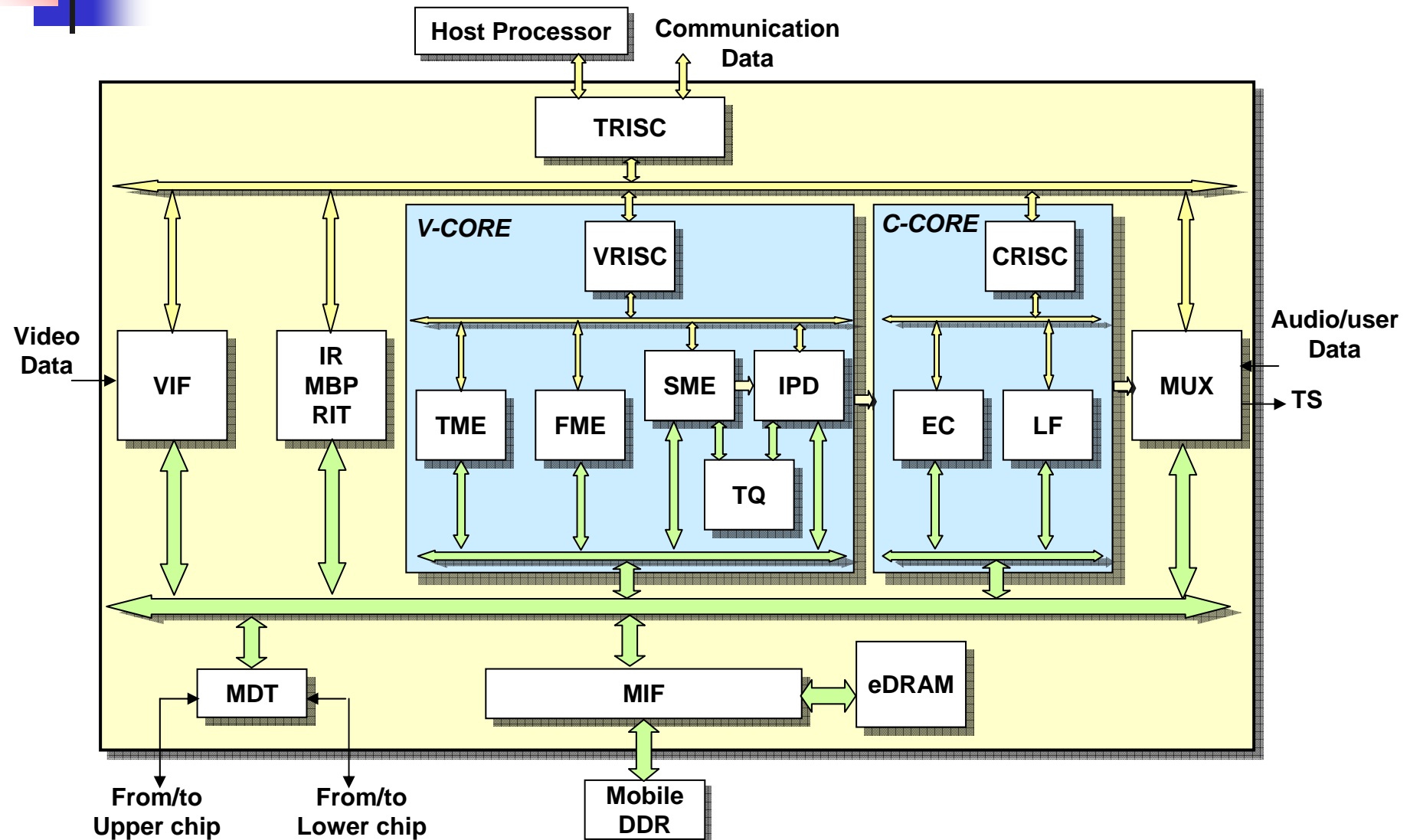
SARA Key Features and Functions

- H.264 high-quality CODEC for professional applications
 - Contribution: 4:2:2, CBR, low-delay and high-bitrate
 - Distribution: 4:2:0, CBR, low-bitrate (high-compression)
 - Storage: 4:2:2/4:2:0, VBR
- Real-time {H.264:MPEG-2} transcoding using recoding information and/or external preprocessing information
- Wide range of coding-modes for efficient encoding and transcoding (CABAC/CAVLC, weighted prediction, variation of multiple reference frames, etc)
- Preprocessing of picture characteristics extraction
- High-precision adaptive hierarchical motion estimation with optimized H.264's mode decision
- Dynamic selective entropy coding (CABAC/CAVLC)

H.264 Algorithms and their Mapping

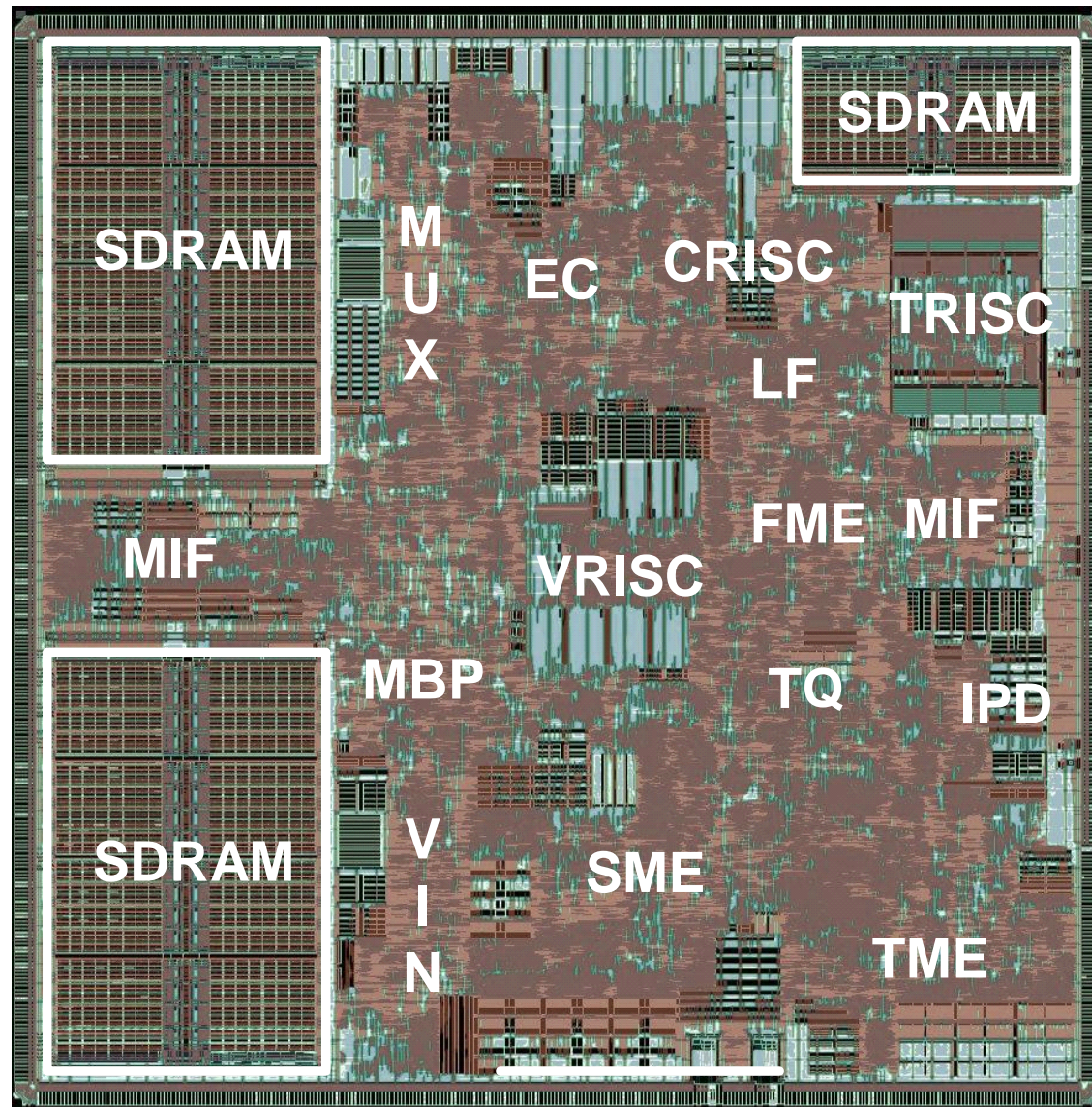


SARA Architecture(Block Diagram)



➔ **Multiple Core Encoding Scheme**

Photograph of SARA





SARA Physical Features

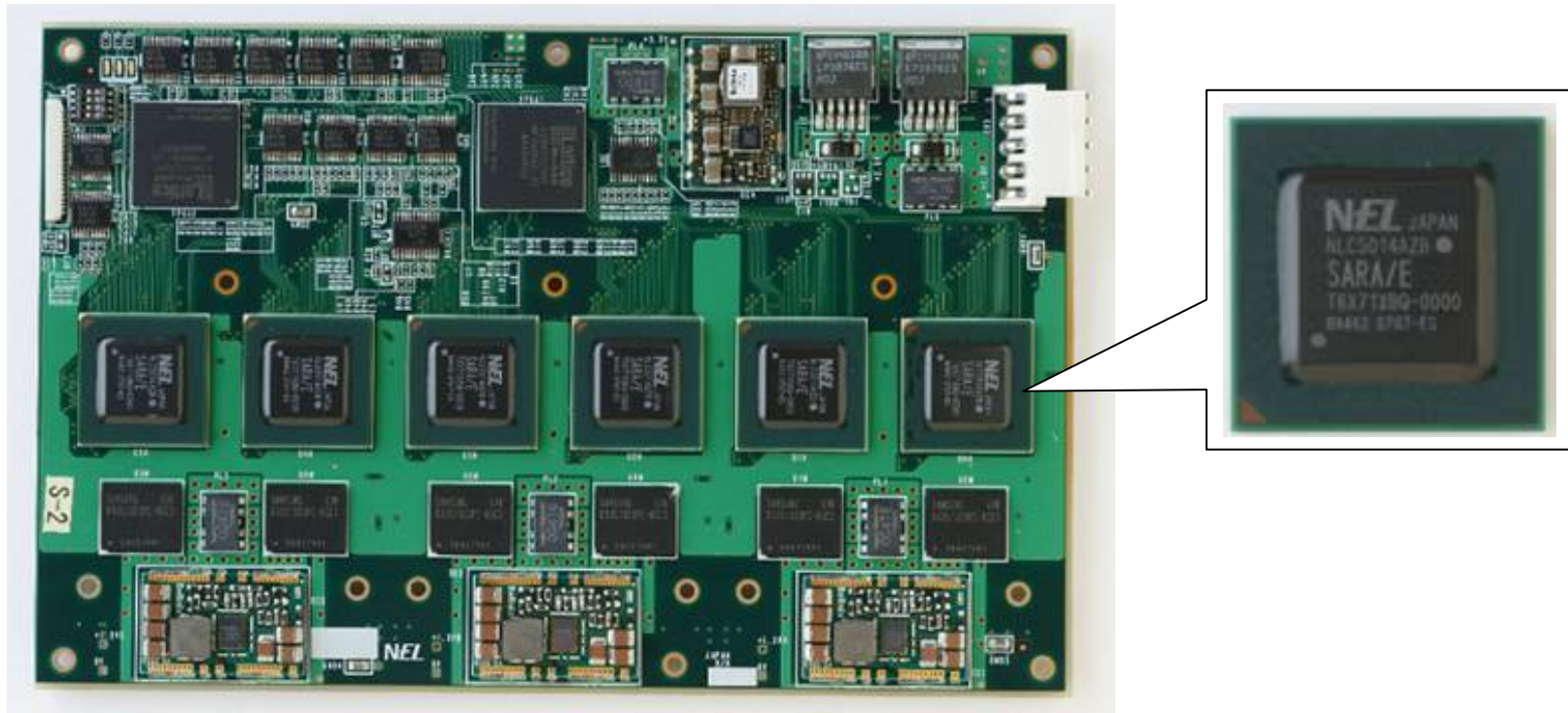
| | |
|------------------------------|-------------------------------------------------------------------|
| Technology | 90nm CMOS |
| Number of transistors | 140 million transistors |
| Clock frequency | 200 MHz/ Max. |
| Supply voltage | Core: 1.2 V / I/O: 3.3 V / eDRAM: 2.5 V / Mobile DDR 1.8 V |
| Power consumption | 3.0 W/ Max. |
| Package | 625-pin FCBGA (21mm x 21 mm) |
| External memories | 512 Mbit (32 bit) Mobile-DDR |



SARA Function Features

| | | |
|---------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Video | Profile and level | Profile: H.264 Main / High / High422(8bit only) Level: 3.0 / 4.0 / 4.1 MPEG-2 {MP, 422P} @ {ML, HL} |
| | Search range | -217.75/+199.75(H), -109.75/+145.75(V) |
| | Resolution and video rate | <i>Encoding:</i> Single-chip: 720 x 480 at up to 30 frames per second Multi-chip: 1920 x 1080 at up to 30 frames per second <i>Decoding:</i> 720 x 480 at up to 30 frames per second 1920 x 1080 at up to 30 frames per second |
| | Transcoding | Combination of H.264/MPEG-2 input and H.264/MPEG-2 output using recoding and/or our original information |
| | Pre-processing | Macroblock based functional filters Macroblock based feature extraction functions |
| Audio | I/O Format | Linear PCM or Encoded stream (AAC) Handling by external audio codec |
| User | I/O Format | PES format for timecode and another audio data |
| System | I/O Format and Bitrate | MPEG-2 TS(188/204 bytes) Max. 120 Mbps |

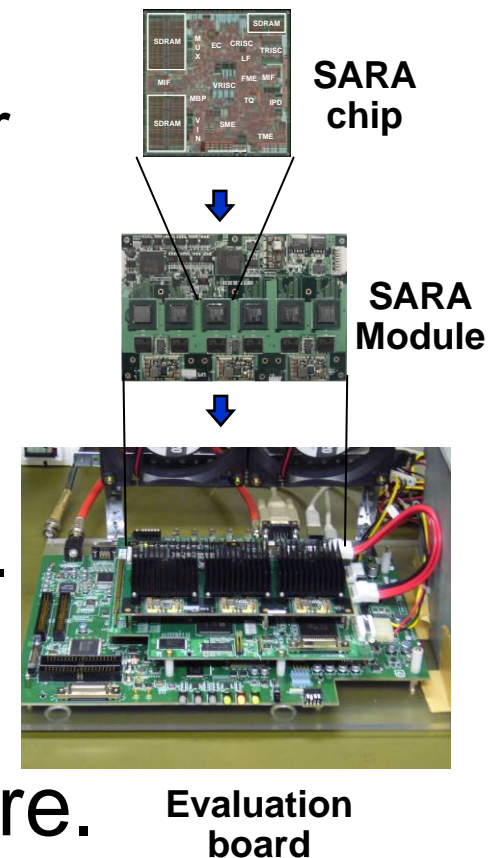
SARA Multi-chip HDTV Module



➡ ***Very Compact Post-card-size HDTV Module
with transcoding capability***

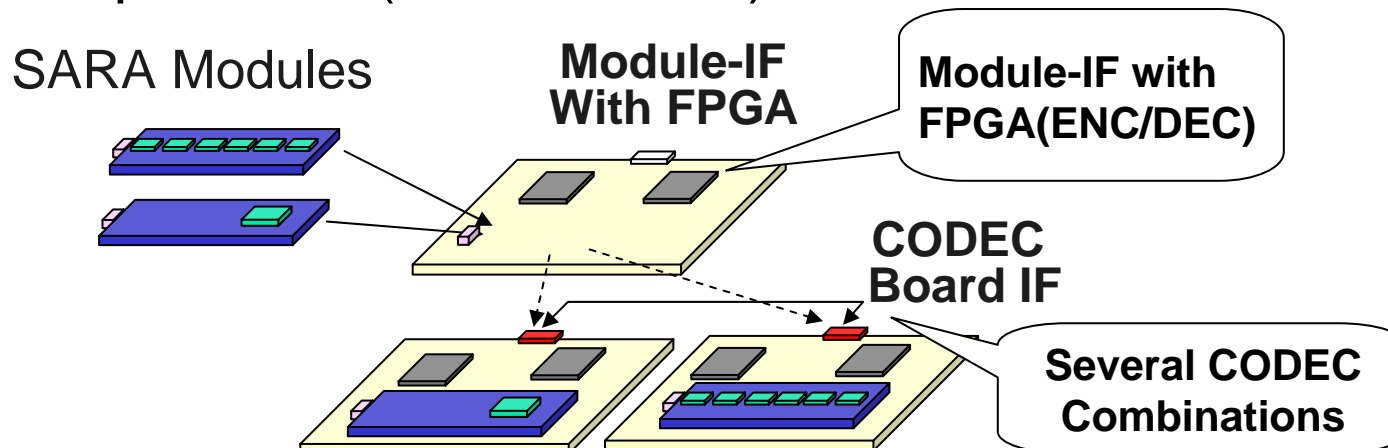
SARA Evaluation and Validation

- Before fabrication,
HW/SW were carefully evaluated and validated using VCS and ASIC emulator through small- and/or full-size images.
 - After fabrication,
HW/SW were evaluated and validated using SARA CODEC evaluation boards.
- ➡ The first silicon is *successfully* implemented with complete software.



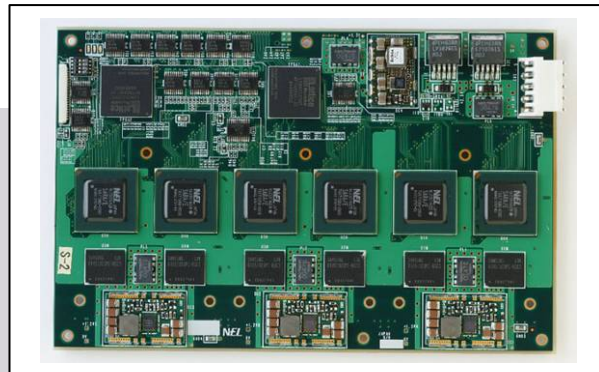
High-end Flexible CODEC Systems

- Very compact post-card-size HDTV modules with transcoding capability.
- Building-block based flexible CODEC systems for various professional applications,
 - MPEG-2/H.264 real-time transcoder for IP based H.264 re-transmission from radio wave broadcasting (MPEG-2),
 - H.264/H.264 real-time transcoder for future complete H.264-based digital TV broadcasting,
 - H.264-based tandem (two-passed) encoding for higher-compression (lower-bitrate) of final distribution.



SARA Flexible CODEC System(1/2)

SARA H.264 (Encoder Module)



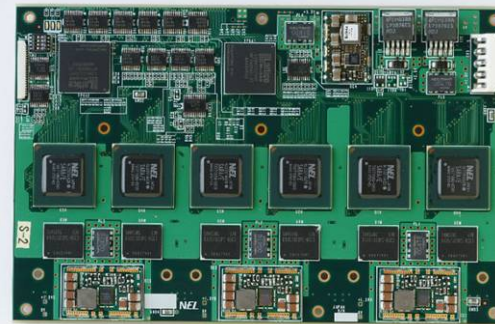
➡ ***SARA High-Quality Encoder System***

SARA Flexible CODEC System(2/2)

VASA MPEG-2
(Decoder Module)



SARA H.264
(Encoder Module)



➡ **SARA MPEG-2/H.264 Transcoder System**



Summary

- Background and Motivation
 - HDTV Broadcast Infrastructure
 - SARA Main Architecture
 - H.264 Algorithms and their Mapping
 - Block Diagram and its MB Pipelined Scheme
 - SARA Implementation
 - Physical & Functional Features
 - SARA High-end Flexible CODEC System
 - High-quality Encoder System
 - MPEG-2/H.264 Transcoder System
- ➔ **SARA** is a **key LSI** for implementing various professional H.264/MPEG-2 applications for future broadcast infrastructure.